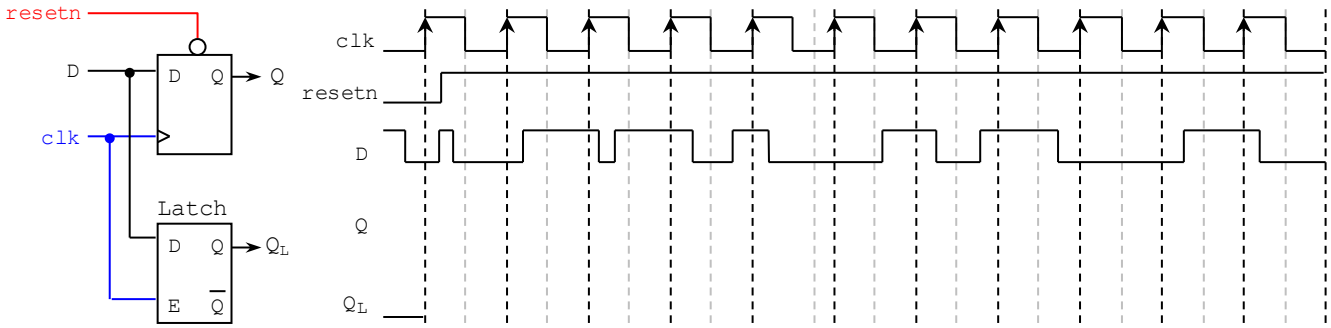
Homework 3

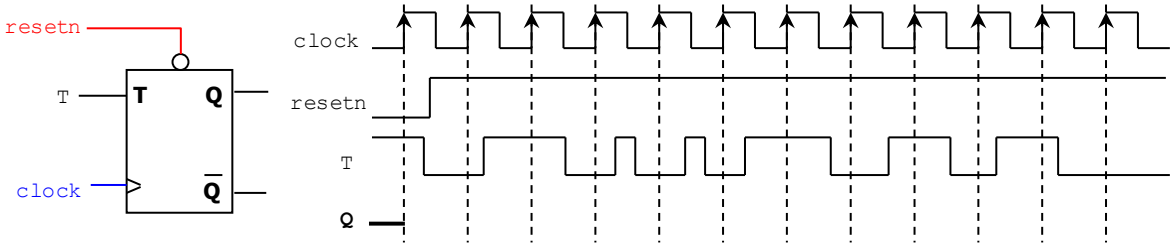
(Due date: November 1st @ 5:30 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (12 PTS)

- Complete the timing diagram for the flip flop and the latch shown below: (7 pts)

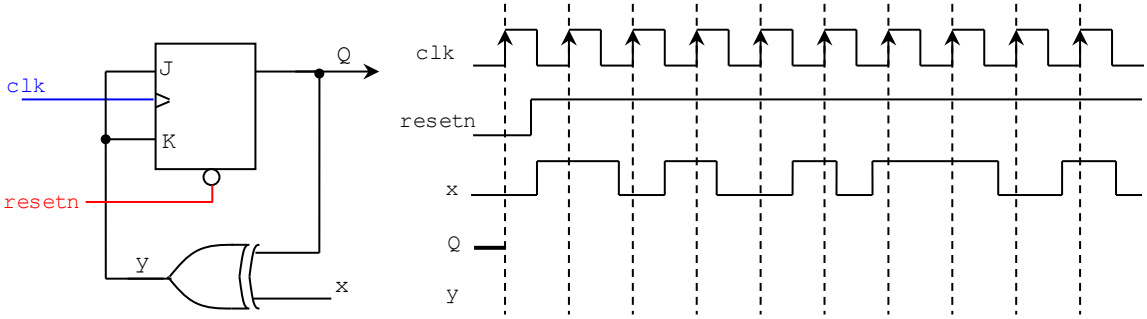


- Complete the timing diagram of the circuit shown below. (5 pts)

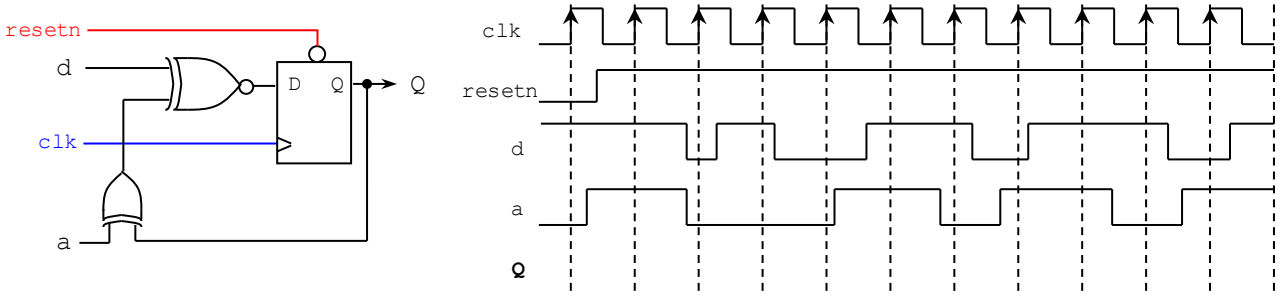


PROBLEM 2 (40 PTS)

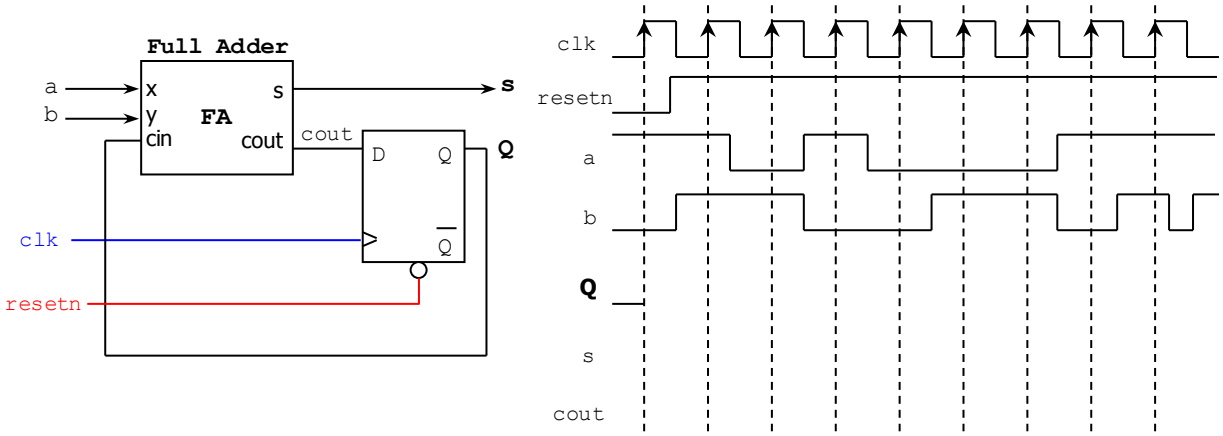
- Complete the timing diagram of the circuit shown below: (7 pts)



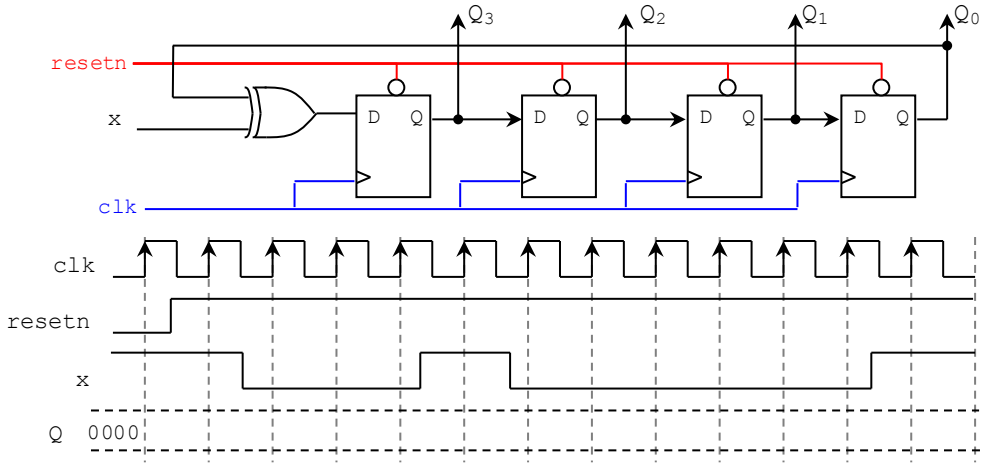
- Complete the timing diagram of the circuit shown below: (8 pts)



- Complete the timing diagram of the circuit shown below: (10 pts)

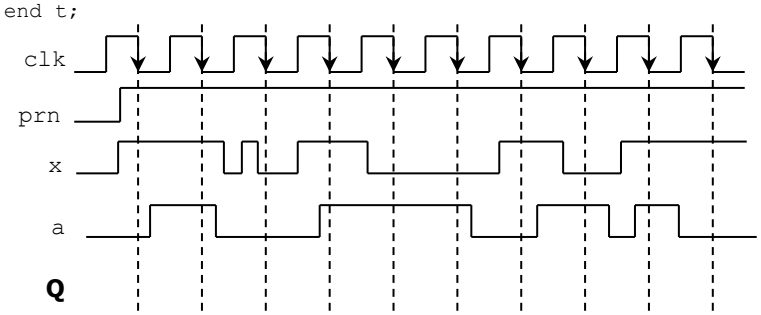


- Complete the timing diagram of the circuit shown below. $Q = Q_3Q_2Q_1Q_0$ (9 pts)



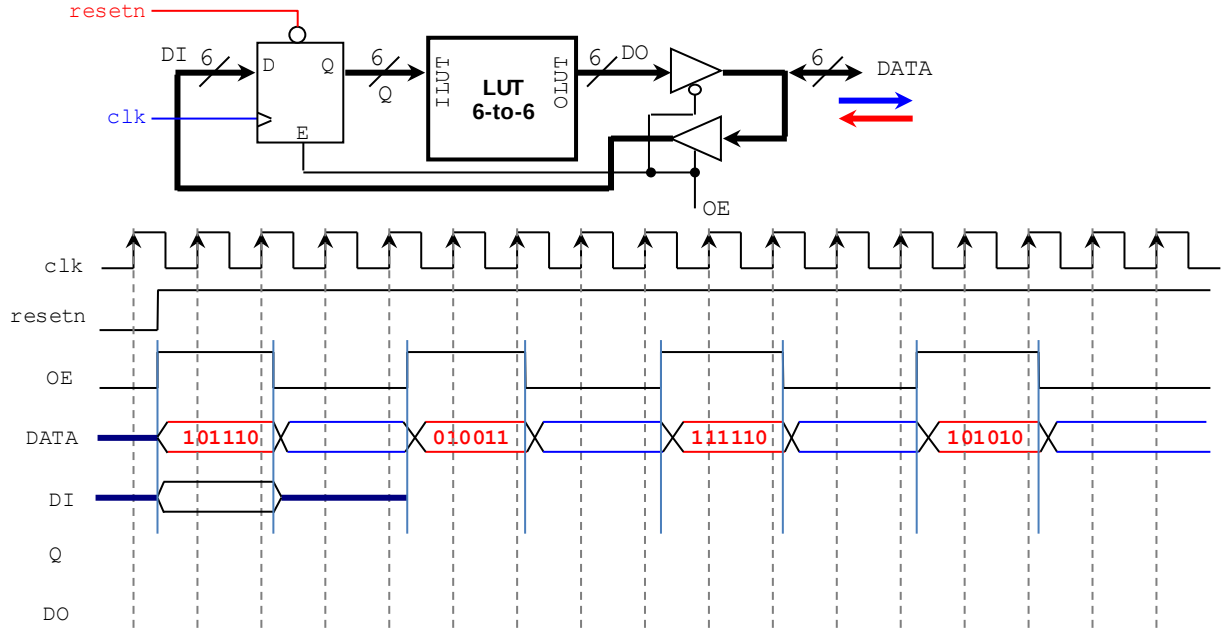
- Complete the timing diagram of the circuit whose VHDL description is shown below: (6 pts)

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port ( prn, a,x,clk: in std_logic;
         q: out std_logic);
end circ;

architecture t of circ is

   signal qt: std_logic;

begin
   process (prn, clk, a, x)
   begin
     if prn = '0' then
         qt <= '1';
      elsif (clk'event and clk = '0') then
         if x = '0' then
             qt <= qt xor not(a);
         end if;
      end if;
   end process;
   q <= qt;
end t;
```



PROBLEM 3 (18 PTS)

- Given the following circuit, complete the timing diagram (signals DO and $DATA$).
  The LUT 6-to-6 implements the following function: $OLUT = \lceil ILUT^{0.79} \rceil$, where $ILUT$ is a 6-bit unsigned number.
  For example $ILUT = 35\ (100011_2) \rightarrow OLUT = \lceil 35^{0.79} \rceil = 17\ (010001_2)$



PROBLEM 4 (30 PTS)

- The following circuit is a 4-bit parallel/serial load shift register with enable input.
  Shifting operation: `s_l=0`. Parallel load: `s_l=1`. Note that $Q = Q_3Q_2Q_1Q_0$. $D = D_3D_2D_1D_0$
  - ✓ Write a structural VHDL code. You MUST create a file for: i) flip flop, ii) MUX 2-to-1, and iii) top file (where you will interconnect the flip flops and MUXes). Provide a printout. (10 pts)
  - ✓ Write a VHDL testbench according to the timing diagram shown below. Complete the timing diagram by simulating your circuit (Behavioral Simulation). The clock frequency must be 50 MHz with 50% duty cycle. Provide a printout. (20 pts)